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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,717	12/15/2005	Freddy Roozeboom	NL 040226	8503

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EXAMINER	
PHINAZEE, SIDNEY S	
ART UNIT	**PAPER NUMBER**
2815	

NOTIFICATION DATE	DELIVERY MODE
08/20/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,717	ROOZEBOOM ET AL.	
	Examiner	Art Unit	
	SIDNEY PHINAZEE	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8-29-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 21, 2008 has been entered.

Response to Arguments

Applicant's arguments filed July 21, 2008 have been fully considered but they are not persuasive. As previously examined, the previous claims do not structurally distinguish over the applied art, particularly where Chudzik shows the “same" dielectric layer material between the trench capacitor electrodes and between a substrate and interconnect layer.

Claim Rejections - 35 USC § 112

Claim 23 is rejected as best understood under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim is unclear as to what units of depth the invention is claiming, which could be any value in centimeters, angstroms or nanometers, etc.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-8, 10, 20-21, 23, 25, and 27 are rejected as best understood under 35 U.S.C. 102(e) as being anticipated by Chudzik et al (US 7,030,481 B2)

1. **Regarding claim 1 Chudzik** an electronic device comprising a semiconductor substrate (200) having a first side and a second side; a vertical trench capacitor (3010) on the first side of the substrate, the vertical trench capacitor (3010) including a plurality of trenches in which dielectric material (3020) is present between first (3030) and second (3080) conductive surfaces; and a vertical interconnect (210, 410', 610') that extends through the substrate extending from the first side to the second side, the vertical interconnect being insulated from the substrate by dielectric material (220, 420'), the dielectric material of the vertical interconnect and the dielectric material (3020) of the vertical trench capacitor being common material formed from a single deposition layer. (fig 3B, 4A, 6)

2. Regarding claim 3 Chudzik discloses an electronic device, characterized in that the vertical interconnect includes a plurality of parallel trenches each of which is substantially filled with electrically conductive material (230,430).

3. Regarding claim 5 Chudzik discloses an electronic device, characterizes contact pads (240, 270) being present. Chudzik does not explicitly state that the contact pads are for coupling to an external carrier that is present on the second side; or that a first vertical interconnect is used for grounding or that a second interconnect is used for signal transmission.

4. Regarding claim 5, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior structure is capable of performing the intended use, then it meets the claim. The applicants intended use of the claimed structure does not structurally distinguish itself over the structure taught by Chudzik. Therefore the recitation of the "a first vertical interconnect is used for grounding" and "second interconnect is used for signal transmission" has not been given patentable weight.

5. Regarding claim 6, Chudzik discloses an electronic device that is characterized in that the first (210) and second (410', 610) interconnect are designed so as to form a coaxial structure.

6. Regarding claim 7 Chudzik discloses an electronic device characterized in that an integrated circuit is defined on the second side of the substrate (See Chudzik column 4 lines 19-22).

7. Regarding claim 8, Chudzik discloses the substrate to comprise a high ohmic zone (Spec column 7 lines 8-19), which is adjacent to the vertical capacitors and acts as a protection against parasitic currents. (See Fig 3C)

8. Regarding claim 10, Chudzik discloses an assembly comprising the electronic device, and a semiconductor device, which semiconductor device (102) is electrically connected to bond pads (270) present on the first side of the substrate.

9. Regarding claim 20, Chudzik discloses wherein the dielectric material (3020) of the vertical trench capacitor and the dielectric material (220, 420') of the vertical interconnect are formed by depositing a layer of dielectric material (220, 420', 3020) on the substrate (200) and partially etching the deposited layer of dielectric material.

10. Regarding claim 21, Chudzik discloses wherein the dielectric material (3020)of the vertical trench capacitor and the dielectric material (220, 420') of the vertical interconnect are identical dielectric material formed from the single deposition layer.

11. Regarding claim 23, Chudzik discloses An electronic device comprising: a semiconductor substrate (200) having a first side and a second side; a plurality of trenches (fig 3B) on the first side of the substrate (200), each of the trenches extending into the substrate from the first side to a depth; conductive material (3030, 3080, 230, 430') lining each of the trenches; a vertical interconnect (210, 410', 610'') that extends through the substrate from the first side to the second side, the vertical interconnect having walls; a single deposition layer of dielectric material on the first and second sides

of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect.

12. Regarding claim 25, Chudzik discloses wherein the vertical interconnect (210, 410', 610") includes a plurality of parallel trenches.

13. Regarding claim 27, Chudzik discloses wherein the plurality of trenches form a vertical trench capacitor (3010).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. **Claims 2, 4, 24, and 26 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Chudzik in view of Kosaki et al (6,268,619).

15. Regarding claim 2 Chudzik disclose the limitations of claim 1 but fails to disclose the limitations of of the vertical interconnect, which first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape. However, Kosaki discloses the vertical interconnect which first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape (3) (see figure 14). It would have been obvious to one having ordinary skill in the art at the time the invention to incorporate the teaching of

Kosaki with that of Chudzik because in this sixth embodiment, the anisotropic dry etching as well as the wet isotropic etching form the opening (3). Therefore, in the vicinity of the front surface of the substrate, the opening has a cylindrical shape so that the substrate is not locally thin, thereby suppressing occurrence of cracks. (See Kosaki column 17 lines 10-15)

16. Regarding to claim 4 Chudzik discloses an electronic device, characterized in that the first part of the vertical interconnect comprises a plurality of parallel through-holes that extend from the first side of the substrate to the second part of the vertical interconnect each of the plurality of parallel through holes being substantially filled with electrically conductive material (230, 430).

17. **Claim 9 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Chudzik in view of Goldberger et al (6,538,300).

18. Regarding claim 9 Chudzik disclose all of the limitations of claim 8 (as discussed above) Chudzik further teaches the high ohmic zone (Spec column 7 lines 8-19). But fails to disclose all limitations of claim 9 that characterizes a planar capacitor that is present on the first side of the substrate, which planar capacitor comprises the same layer of dielectric material as the vertical capacitor. However, Goldberger discloses an electronic device, characterized in that a planar capacitor is present on the first side of the substrate, which planar capacitor (10) comprises the same layer of dielectric

material (104) as the vertical capacitor. It would have been obvious to one having ordinary skill in the art at the time the invention to incorporate the teaching of Goldberger with that of Chudzik because capacitors in accordance with Goldberger's invention exhibit numerous advantages. For example, they can be fabricated at a wafer level with a very low effective series resistance (ESR). (See Goldberger column 1 paragraph 8).

19. **Claim 22, 24, and 26 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Chudzik in view of Hsuan et al (2001/0005046 A1).

20. Regarding claim 22 Chudzik disclose all of the limitations of claim 1, (as discussed above). Chudzik further teaches wherein the vertical interconnect (210, 410', 610'') is substantially filled with conductive material (230, 430', 630''), the conductive material of the vertical interconnect and the second conductive (3080) surface of the vertical trench capacitor; but fails to teach the invention being formed from common material of a single deposition layer of conductive material.

21. However Hsuan teaches the conductive material of the "vertical interconnect" (46) being formed of the common material layer of the trench capacitor's second conductive surface. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a common material, since it has been held to be within the general skill of worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416

22. Regarding claim 24, Chudzik discloses the limitation of claim 23 (addressed above). Chudzik further teaches wherein the vertical interconnect (210, 410', 610'') has a first part and a second part, the first part extending from the first side of the substrate (200) to the second part, the second part extending from the second side of the substrate to the first part but fail to teach the second part being wider than the first part.

23. However Hsuan teaches the second part (52 in fig 2G) being wider than the first part. It would have been an obvious matter of design choice to use a specific size, since such modification would have involved mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955)

24. Regarding claim 26 Chudzik in view of Hsuan discloses the limitation of claim 24 (addressed above). Chudzik further teaches wherein the first part of the vertical interconnect (210, 410', 610'') includes a plurality of parallel trenches each of which extends from the first side of the substrate (200) to the second part of the vertical interconnect.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIDNEY PHINAZEE whose telephone number is (571)270-5020. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth A Parker/
Supervisory Patent Examiner, Art Unit 2815

/SSP/